REMARKS

The present invention is a tuning circuit and a method of controlling a tuning circuit. In accordance with an embodiment of the invention, a tuning circuit comprises a first reactance 12 and 42, a second reactance 13 and 43, and an insulated gate field effect transistor 11 having a gate arranged to receive a control signal, the first reactance being connected between the source of the field effect transistor and a first node and the second reactance having the same value as the first reactance and being connected between the drain of the first field effect transistor and the second node, and wherein the first and second nodes are arranged so as to experience a balanced ac signal and there being no circuit connection for grounding the source and drum of said transistor. See Fig. 1 and Figs.6a-6d.

The Examiner's allowance of claims 14-39 is noted with appreciation.

Claims 1, 2, 4, and 5 stand rejected under 35 U.S.C. §102 as being anticipated by United States Patent 6,239,665 (Strom). With respect to claims 1, 2, 4 and 5, the Examiner reasons as follows:

Re claims 1-2, Strom teaches a tuning circuit comprising (Fig.1A):

a first capacitor (118), a second capacitor (112), and an insulated gate field effect transistor (136) having a gate to receive a control signal, the first capacitor being connected between the source of the field effect transistor and a first node and the second capacitor having the same value as the first capacitor and being connected between the drain of the field effect transistor and a second node, wherein the first and second nodes are arranged so as to experience a balanced ac signal.

Re claim 4, Strom teaches a capacitor (114 & 116) connected between said nodes.

Re claim 5, Strom teaches an inductor (108 & 110) connected between said nodes.

These grounds of rejection are traversed for the following reasons:

Strom discloses an oscillator circuit which is tuned by the use of field effect transistors which are switched to connect together reactances such as capacitances 112 and 118 and 114 and 116 by respectively turning on field effect transistors 142 and 136. Shunt field effect transistors 138 and 140 shunt the capacitors 112 and 118 to ground upon application of the control signal S1 and field effect transistors 132 and 134 shunt capacitors 114 and 116 to ground upon application of control signal S0. It is noted that with respect to the coupling together of capacitors 114 and 116 that field effect transistors 132, 134 and 136 are all turned on by the signal S0 and the coupling together of capacitors 112 and 118 is accomplished by turning on the transistors 138, 140 and 142 by the application of the control signal S1.

Independent claim 1 recites, *inter alia*, "there being no circuit connection for grounding the source and drain of said field effect transistor" which is distinct from the operation of the field effect transistors 136 and 142 in the embodiments of Figs. 1a and 1b. The capacitors and inductors are shunted to ground upon the application respectively of the control signals S0 and S1 to the field effect transistors coupled thereto by causing the field effect transistors to be turned on.

Moreover, there is no basis why a person of ordinary skill in the art would be led to modify the teachings of Strom to provide a topology in which there is no grounding of the source and drain of the field effect transistor as recited in claim 1.

Dependent claims 2, 4 and 5 are patentable for the same reasons set forth above with respect to claim 1. Moreover, it is requested that the Examiner consider the withdrawal of claim 3 from consideration in view of its dependency from claim 1 which is submitted to be neither anticipated nor rendered obvious by Strom.

Newly submitted method claims 43-45 recite a method of controlling a tuning circuit which, *inter alia*, recites "turning on said field effect transistor during control of the tuning circuit while at the same time maintaining the source and drain of said field effect transistor isolated from ground." This subject matter has no counterpart in Strom for the reasons explained above that the source and drain of the field effect transistors 136 and 142 are grounded when the control signals S0 and S1 are applied with a signal level to turn on the field effect transistors 136 and 142.

Therefore, an operation occurs in which the source and drain of the field effect transistors are grounded. There is no basis in the record why a person of ordinary skill in the art, as stated above with respect to claim 1, would modify Strom to provide an ungrounded mode of operation. Dependent claims 44 and 45 are patentable for the same reasons set forth above.

In view of the foregoing amendments and remarks, it is submitted that each of the claims in the application is in condition for allowance. Accordingly, early allowance thereof is respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 C.F.R. §1.136. Please charge any shortage in fees due in connection with the

filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (1076.40408VX1) and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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Attachments

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